IN THE SPECIFICATION

Please replace the paragraph starting on page 20, line 13 with the following amended paragraph:

Figure 5 is a timing diagram containing various signals (generated within tracking circuit 399) illustrating the generation of a latch enable signal in an appropriate window according to an aspect of the present invention. The timing diagram is shown containing clock signal 510 ~~(generated by clock generator 320)~~, pulse out 515 (generated by pulse generator 330), set output 520 (generated by S/R latch 350), sense enable 530 (generated by inverter 360), V401 540 (voltage at node 401), V421 550 (voltage at node 421), V389 560 (voltage at node 389), and latch enable 580 (generated by latch enable generator 390).